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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,522	07/24/2002	William Mar	VIAP0043USA	6635

27765 7590 11/14/2005

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EXAMINER	
PANWALKAR, VINEETA S	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/064,522	MAR, WILLIAM	
	Examiner	Art Unit	
	Vineeta S. Panwalkar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 6 January 2005 has been considered in view of the letter submitted by applicant on 6 January 2005; i.e. it has been assumed (taking the corresponding figures into consideration) that US patent 3,997,773 and EPO publication EP0601605 are the English language are counterparts to Japanese Application Numbers 51-55650 and 06-232933 respectively.

Specification

3a. The abstract of the disclosure is objected to as to minor informalities. It is suggested that the title of the invention " [Multi-interpolated data recovery with a relative low sampling rate] " be removed from the abstract. Correction is required. See MPEP § 608.01(b).

3b. Page 19 of 26 with the title "Figures" should be removed, as it is a blank page.

3c. The disclosure is objected to because of the following informalities:

- The title of the invention " [Multi-interpolated data recovery with a relative low sampling rate] " should be replaced by --- Multi-interpolated data recovery with a relative low sampling rate--- i.e. the square brackets "[" and "]" should be removed. Appropriate correction is required.

Claim Objections

4. Claim 11 is objected to as to minor informalities. It is suggested that "interpolatorrespectively" in line 11 of the claim be replaced by --- interpolator respectively---. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-10, 14 and 17-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 1, 6,14 and 17, it is unclear from the specification what is meant by the limitation "wherein the sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of the data clock". Particularly, in view of Fig. 6, it appears as if the claimed sampling frequency is lower than the maximum frequency of the input signal bandwidth. Even though Fig. 4 shows the frequencies as claimed, the relationship between data clock frequency and maximum frequency of the signal seems unclear from the disclosure. In paragraph [0027] on page 7 of the specification, it is unclear by what is meant by "As shown in Fig. 1, after the coding modulation of the original signal, the rate of change of an original signal waveform 10 is slower than the rate of change of a data clock 12. For instance, as the data clock 12 experiences one period, the waveform of original signal 10 only increases leisurely from time t1 to t2".

It has been disclosed in paragraphs [0007] and [0008] on pages 2 and 3 respectively of the specification, it has been mentioned that the data clock is not available for use. In paragraph [0008], it is further mentioned that because the data clock is unavailable, the sampling clock of the recovery circuit is not synchronized with the data clock. Since the data clock is unavailable, it is unclear how it can be determined whether the claimed sampling frequency is higher or lower than the data clock.

Claims 2-5,7-10 and 18-20 are rejected as being dependent on rejected base claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 11-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 11, it is unclear from the claim language what is meant by " a computation module responsive to an output signal for calculating a plurality of control words during each sampling period", since it has not been further clarified where the claimed output comes from.

Claims 12-16 are rejected under 35 U.S.C. 112, second paragraph as being dependent upon claim 11.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's own admitted prior art, hereinafter AOAPA, in view of Lipka (US 6459743 B1), hereinafter Lipka.

Rejections are based on the assumption that the sampling frequency is lower than the maximum frequency of the input signal bandwidth.

7a. Regarding claim 1, AOPA discloses a data recovery method for recovering digital data from a corresponding input signal, the digital data being synchronized with a data clock, the data clock comprising a plurality of data periods, amplitude of the input signal during each data period of the data clock representing the digital data (Circuit of Fig. 2 performs this method; see Figs. 1,2 and 3 and paragraphs [0007] – [0012] of the specification;); the data recovery method comprising:

- selecting a sampling clock with a predetermined sampling frequency, the sampling clock comprising a plurality of sampling periods (Performed by unit 23 of Fig.1);
- calculating at least a control word during each sampling period, each control word being used for estimating a phase error between the sampling period and the corresponding data period (Performed by unit 26 of Fig.1);
- calculating an original amplitude of the input signal within each data period of the data clock according to the corresponding control word and amplitude of the input signal during each sampling period of the sampling clock for recovering the digital data; and storing the original amplitude of the input signal of the corresponding control word (See paragraphs [0010] and [0011] of specification; the computation module inherently stores the control word);

However, the sampling frequency of the AOAPA is higher than the maximum frequency bandwidth.

However, in the same filed of endeavor, Lipka discloses a digital reception with frequency sampling wherein:

- wherein the sampling frequency is lower than the maximum frequency of the input signal bandwidth (Column 4, lines 49-56).

Thus, it would be obvious to use the under-sampling method suggested by Lipka as his method claims that the subsequent interpolation achieves proper alignment for any timing errors that may arise (Column 8, lines 12-17).

7b. Regarding claim 2, AOAPA further discloses data recovery method wherein :

- control word is calculated according to the amplitude of the input signal during the corresponding sampling period (See paragraph [0009] of specification).

7c. Regarding claim 3, AOAPA further discloses data recovery method wherein:

- the input signal is outputted from an optical disk storage device, such as a compact disk (CD) player, CD- ROM or digital versatile disc (DVD) device (See paragraph [0004] of specification).

7d. Regarding claim 4, AOAPA further discloses data recovery method wherein:

- the step of using the recovered digital data to adjust the control word further (Fig. 2, output signal is fed back to compute control word and hence is

interpreted as the claimed using of the recovered digital data to adjust the control word further).

7e. Regarding claim 5, AOAPA further discloses data recovery method wherein:

- a weighted interpolation algorithm is used for calculating the original amplitude of the input signal during each data period according to the corresponding control words and amplitude of the input signal during each sampling period. (See paragraph [0010] of specification).

7f. Regarding claim 6, AOPA discloses a data recovery circuit for recovering digital data from a corresponding input signal, the digital data being synchronized with a data clock, the data clock comprising a plurality of data periods, amplitude of the input signal during each data period of the data clock representing the digital data (Circuit of Fig. 2; see Figs. 1,2 and 3 and paragraphs [0007] – [0012] of the specification); the data recovery circuit comprising:

- a sampler for measuring amplitude of said input signal during each sampling period, a duration of each sampling period being fixed and being related to a sampling frequency (Fig. 2, unit 23);
- a computation module for calculating at least a control word during each sampling period, each control word being used for estimating a phase error between said sampling period and the corresponding data period (Fig. 2, unit 26);

- and at least an interpolator, each interpolator respectively handling each control word during one sampling period for calculating each amplitude of said input signal during each data period according to both the corresponding control word and an output of the sampler in order to recover said digital data (Fig. 2, unit 24);

However, the sampling frequency of the AOAPA is higher than the maximum frequency bandwidth.

However, in the same filed of endeavor, Lipka discloses a digital reception with frequency sampling wherein:

- wherein the sampling frequency is lower than the maximum frequency of the input signal bandwidth (Column 4, lines 49-56).

Thus, it would be obvious to use the under-sampling method suggested by Lipka as his method claims that the subsequent interpolation achieves proper alignment for any timing errors that may arise (Column 8, lines 12-17).

7g. Regarding claim 7, AOAPA further discloses data recovery circuit comprising:

- a storage medium connected to said interpolator to receive said amplitude of said input signal within each of said data clock period and to generate the recovered digital data (the computation module inherently stores the control word);

7h. Regarding claim 8, AOAPA further discloses data recovery circuit wherein:

- the control word is calculated according to the amplitude of said input signal during the corresponding sampling period (See paragraph [0009] of specification).

7i. Regarding claim 9, AOAPA further discloses data recovery circuit wherein:

- the computation module uses the recovered digital data to adjust the control word further (Fig. 2, output signal is fed back to compute control word and hence is interpreted as the claimed using of the recovered digital data to adjust the control word further).

7j. Regarding claim 10, AOAPA further discloses data recovery circuit wherein:

- interpolator uses a weighted interpolation algorithm for calculating the original amplitude of the input signal during each data period according to the corresponding control words and amplitude of the input signal during each sampling period(See paragraph [0010] of specification).

8. Claims 1- 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's own admitted prior art, hereinafter AOAPA, in view of Urkowitz, "Parallel Realizations of Digital Filters for Increasing the Sampling Rate", IEEE Transactions on Circuits and Systems, VOL. CAS-22, No.2, February 1975, pp 146-154, hereinafter referred to as Urkowitz.

Rejections for claims 1-10 and claim 14 are based on the assumption that the 35 U.S.C. 112, first paragraph made above in paragraph 5 will be overcome by providing a proper explanation and without the addition of new matter. In light of the specification, it is also assumed that the claimed limitation "wherein the sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of the data clock" is obtained merely by using a plurality of interpolators in parallel.

8a. Regarding claim 1, AOPA discloses a data recovery method for recovering digital data from a corresponding input signal, the digital data being synchronized with a data clock, the data clock comprising a plurality of data periods, amplitude of the input signal during each data period of the data clock representing the digital data (Circuit of Fig. 2 performs this method; see Figs. 1,2 and 3 and paragraphs [0007] – [0012] of the specification); the data recovery method comprising:

- selecting a sampling clock with a predetermined sampling frequency, the sampling clock comprising a plurality of sampling periods (Performed by unit 23 of Fig.1);
- calculating at least a control word during each sampling period, each control word being used for estimating a phase error between the sampling period and the corresponding data period (Performed by unit 26 of Fig.1);
- calculating an original amplitude of the input signal within each data period of the data clock according to the corresponding control word and amplitude of

the input signal during each sampling period of the sampling clock for recovering the digital data; and storing the original amplitude of the input signal of the corresponding control word (See paragraphs [0010] and [0011] of specification);

However, the sampling frequency of the AOAPA is higher than the data clock frequency.

However, in the same filed of endeavor, Urkowitz discloses a parallel realization of digital interpolation filters wherein:

- wherein the sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of the data clock (Fig. 2 shows how interpolators may be used in parallel. Section IV on pages 148-150 explains the parallel realization).

Thus, it would be obvious to use the parallel interpolation filter realization as disclosed by Urkowitz because it simplifies the arithmetic involved (Abstract).

8b. Claims 2-5 are rejected using AOAPA as shown in paragraphs 7b-7e above.

8c. Claim 6 is with a corresponding circuit version of the rejection for claim1 in paragraph 8s above.

8d. Claims 7-10 are rejected using AOAPA as shown in paragraphs 7g-7j above.

8e. A data recovery circuit for recovering digital data with a relative low sampling frequency, the data recovery circuit comprising (Circuit of Fig. 2; see Figs. 1,2 and 3 and paragraphs [0007] – [0012] of the specification):

- a sampling device for sampling an analog input signal to generate a sequence of discrete time sample values that represent amplitudes of said input signal during each sampling period, a duration of each sampling period being fixed and being inversely related to said sampling frequency (unit 23 of Fig.1);
- a computation module responsive to an output signal for calculating a control word during each sampling period, said control word being used for estimating a phase error between said sampling period and a data clock period (unit 26 of Fig.1 calculates a control word);
- a plurality of interpolators, each interpolator respectively handling each of said control words during one sampling period together with each of said discrete time sample values for calculating an amplitude of said input signal within each of said data clock period in order to recover said digital data.

However, the sampling frequency of the AOAPA does not disclose plurality of interpolators and control words per sampling period.

However, in the same filed of endeavor, Urkowitz discloses a parallel realization of digital interpolation filters wherein:

a plurality of interpolators, each interpolator respectively handling each of said control words during one sampling period together with each of said discrete time sample values for calculating an amplitude of said input signal within each of said data clock period in order to recover said digital data (Fig. 2

shows how interpolators may be used in parallel. Section IV on pages 148-150 explains the parallel realization).

- a computation module responsive to an output signal for calculating a plurality of control words during each sampling period, said control words being used for estimating a phase error between said sampling period and a data clock period (Thus it is obvious that unit 26 of Fig.1 will calculate plurality of control words if a plurality of interpolators exist);

Thus, it would be obvious to use the parallel interpolation filter realization as disclosed by Urkowitz because it simplifies the arithmetic involved (Abstract).

8f. Regarding claim 12, Urkowitz further implies that :

- said computation module comprises a plurality of computation units for generating said plurality of control words (It is obvious that unit 26 of Fig.1 will calculate plurality of control words using plurality of computation units if a plurality of interpolators are used).

Thus, it would be obvious to use the parallel interpolation filter realization as disclosed by Urkowitz because it simplifies the arithmetic involved (Abstract).

8g. Regarding claim 12, Urkowitz further implies that:

- said sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of said

data clock ((Fig. 2 shows how interpolators may be used in parallel. Section IV on pages 148-150 explains the parallel realization).

Thus, it would be obvious to use the parallel interpolation filter realization as disclosed by Urkowitz because it simplifies the arithmetic involved (Abstract).

8h. Regarding claim 14, AOAPA further discloses data recovery circuit wherein:

- said sampling frequency, in a frequency domain, is higher than a maximum frequency of the input signal bandwidth and is lower than a frequency of said data clock ((Fig. 2 shows how interpolators may be used in parallel. Section IV on pages 148-150 explains the parallel realization).

Thus, it would be obvious to use the parallel interpolation filter realization as disclosed by Urkowitz because it simplifies the arithmetic involved (Abstract).

8i. Regarding claim 15, AOAPA further discloses data recovery circuit wherein:

- the control word is calculated according to the amplitude of said input signal during the corresponding sampling period (See paragraph [0009] of specification).

8j. Regarding claim 16, AOAPA further discloses data recovery method wherein:

- a weighted interpolation algorithm is used for calculating the original amplitude of the input signal during each data period according to the

corresponding control words and amplitude of the input signal during each sampling period. (See paragraph [0010] of specification).

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over AOAPA, in view of Urkowitz as applied to claim 11 above, and further in view of Lipka based on the assumption that the sampling frequency is lower than the maximum frequency of the input signal bandwidth.

Lipka discloses a digital reception with frequency sampling wherein:

- wherein the sampling frequency is lower than the maximum frequency of the input signal bandwidth (Column 4, lines 49-56).

Thus, it would be obvious to use the under-sampling method suggested by Lipka as his method claims that the subsequent interpolation achieves proper alignment for any timing errors that may arise (Column 8, lines 12-17).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Wu (US 6329859 B1) discloses a circular interpolator system.
- Samueli et al. (US 6498823 B1) disclose variable rate modulator with plurality of interpolators in series.
- Girardi et al. (US 4379347) disclos a receiver with plurality of interpolators.

- Frenkel et al. (US 20020150153 A1) disclose a modem with plurality of interpolators.
- Marzalek et al. (US 4928251) disclose a method and apparatus for waveform reconstruction wherein sampling frequency is lower than Nyquist rate.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VP

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PRIMARY EXAMINER